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Docket No.: YOR91995137X (20140-00235-US1) (PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Panayotis C. Andricacos et al.

Application No.: 10/773,434

Filed: February 9, 2004

For:

ELECTROPLATED INTERCONNECTION

STRUCTURES ON INTEGRATED CIRCUIT

CHIPS

Confirmation No.: Not Yet Assigned

Art Unit: Not Yet Assigned

Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits as far as is known to the undersigned (37 CFR 1.97(b)(3)).

Those patent(s) or publication(s) which are marked with a double asterisk (**) next to the Cite No. in the attached form PTO/SB/08 (facsimile) are not supplied because they were previously cited by or submitted to the Office in a prior application number 09/348,632, filed July 6, 1999 and relied upon in this application for an earlier filing date under 35 U.S.C. 120.

Application No.: 10/773,434

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(20140-00235-US1)

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0510, under Order No. 20140-00235-US1. A duplicate copy of this paper is enclosed.

Dated: /2 may 2004

Respectfully submitted,

urton A. Ameriick

Registration No.: 24,852

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PTO/SB/08a/b (QB-03)

Approved for use through 07/31/2003. OMB 0651-0031

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Substitute for form 1449A/B/PTO		Complete if Known			
Gubsi	DIGITE IOI IOINI 144370001			Application Number	10/773,434
INFORMATION DISCLOSURE				Filing Date	February 9, 2004
STATEMENT BY APPLICANT			PLICANT	First Named Inventor	Panayotis C. Andricacos
				Art Unit	N/A
	(Use as many s	heets as ne	cessery)	Exeminer Name	Not Yet Assigned
Sheet	1	of	2	Attorney Docket Number	20140-00235-US1

			U.S. PA	TENT DOCUMENTS		
Examiner Initials*	Cite	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or	Pages, Columns, Lines, Where Relevant Passages or Relevant	
	No.1	Number-Kind Code ⁹ (If known)		Applicant of Cited Document	Figures Appear	
	AA**	US-3,328,273-A1	06/1967	Creutz et al.		
	AB**	US-3,652,442-A1	03/1972	Powers et al.		
	AC**	US-3,770,598-A1	11/1973	Creutz		
	AD**	US-4,110,176-A1	08/1978	Creutz et al.		
	AE**	US-4,339,319-A1	07/1982	Aigo		
	AF**	US-4,376,685-A1	03/1983	Watson		
	AG**	US-4,555,315-A1	11/1985	Barbieri et al.		
	AH**	US-4,975,159-A1	12/1990	Dahms		
	Al**	US-5,256,274-A1	10/1993	Poris		
	AJ**	US-5,266,446-A1	11/1993	Chang et al.		
	AK**	US-5,312,532-A1	05/1994	Andricacos et al.		
	AL**	US-5,391,517-A1	02/1995	Gelatos et al.		
	AM*	US-5,516,412-A1	05/1996	Andricacos et al.		
	*					
	AN™	US-5,602,423-A1	02/1997	Jain		
	A0**	US-5,635,423-A1	06/1997	Huang et al.		

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No.'	Foreign Patent Document Country Code ³ -Number*-Kind Code ⁶ (If known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevent Passages or Relevent Figures Appear	T ^g		

*EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. "*CITE NO.: Those patent(s) or publication(s) which are marked with an double asterisk ("") next to the Cite No. are not supplied because they were previously clied by or submitted to the Office in a prior application refled upon in this application for an earlier filling date under 35 U.S.C. 120. Applicant's unique citation designation number (optional). *See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. *Enter Office that issued the document, by the two-latter code (WIPO Standard ST.3). *For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. *Kind of document by the appropriate symbols as Indicated on the document under WIPO Standard ST. 16 if possible. *Applicant is to place a check mark here if English language Translation is attacted. attactvod.

		NON PATENT LITERATURE DOCUMENTS				
Examiner Initials	er Cite No.1 Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publishe and/or country where published.					
	CA**	F.A. Lowenheim, "Electroplating", McGraw-Hill Book Co., New York pp. 198-202, 1978.	L			
	CB**	H. Silman et al., "Protective and Decorative Coatings for Metals", Finishing Publications Ltd., Teddington, Middlesex, England, pp. 310-314, 1978.				
	CC**	Bulkeley, Debra, "The First Copper-Based IC's Debut", Design News, Semiconductors, June 7, 1999, pp. S-11-S14.				
	CD**	Andricacos, Panos C., "Copper On-Chip Interconnections, A Breakthrough in Electrodeposition to Make Better Chips", The Electrochem. Soc. Interface, Spring, 1999, pp.32-37.				

Examiner		Date	1
Signature		Considered	
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Substitute for form 1449A/B/PTQ				Complete if Known		
444556	3101101111111442244	-1 14		Application Number	10/773,434	
INFO	DRMATIC	ON DIS	CLOSURE	Filing Date	February 9, 2004	
STATEMENT BY APPLICANT			PPLICANT	First Named Inventor	Panayotis C. Andricacos	
(Use as many sheets as necessary)				Art Unit	N/A	
				Examiner Name	Not Yet Assigned	
Sheet	2	of	2	Altorney Docket Number	20140-00235-US1	

CE** Hirano, Makato et al., "Three Dimensional Passive Elements for Compact GaAs MMICs, IEIC				
1	Transactions on Electronics, vol. E76-C, No. 6, June 1993, pp. 961-967.			
CF**	Contolini et al, "Electrochemical Planarization for Multilevel Metallization", J. Electrochem.			
l	Soc., vol. 141, No. 9, Sep. 1994, pp 2503-2510.	•		

^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 603. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. **CITE NO.: Those patent(s) or publication(s) which are marked with an double asterisk (**) next to the Cite No. are not supplied because they were previously cited by or submitted to the Office in a prior application relied upon in this application for an earlier filing date under 35 U.S.C. 120.

^{&#}x27;Applicant's unique citation designation number (optional). 'Applicant is to place a check mark here if English language Translation is attached.